

Origami-enabled deformable silicon solar cells

Rui Tang,¹ Hai Huang,¹ Hongen Tu,² Hanshuang Liang,¹ Mengbing Liang,¹ Zeming Song,³ Yong Xu,² Hanqing Jiang,^{3,a)} and Hongyu Yu^{1,4,b)}

¹*School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, Arizona 85287, USA*

²*Electrical and Computer Engineering, Wayne State University, 5050 Anthony Wayne Dr., Detroit, Michigan 48202, USA*

³*School for Engineering of Matter, Transport and Energy, Arizona State University, Tempe, Arizona 85287, USA*

⁴*School of Earth and Space Exploration, Arizona State University, Tempe, Arizona 85287, USA*

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Deformable electronics have found various applications and elastomeric materials have been widely used to reach flexibility and stretchability. In this Letter, we report an alternative approach to enable deformability through origami. In this approach, the deformability is achieved through folding and unfolding at the creases while the functional devices do not experience strain. We have demonstrated an example of origami-enabled silicon solar cells and showed that this solar cell can reach up to 644% areal compactness while maintaining reasonable good performance upon cyclic folding/unfolding. This approach opens an alternative direction of producing flexible, stretchable, and deformable electronics. © 2014 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4866145>]

Flexible and stretchable electronics, under an umbrella of macroelectronics, are coming to revolutionize the functionality of microelectronics seamlessly with their application environment, ranging from various consumer electronics to bio-medical applications. Many researchers have studied flexible and stretchable electronics, using various approaches and a wide variety of devices have been fabricated.¹⁻⁴ Among these approaches, one way is to directly fabricate electronic devices on flexible substrate through low-temperature processes and systems such as flexible printed circuit boards (PCBs), thin film transistors (TFTs), and microwave components on flexible substrates have been fabricated.⁵ Recently, an innovative transfer printing approach has been extensively used in flexible and stretchable electronics, where the fabricated functional devices on hard and planar substrates using standard processes are transferred by elastomeric stamps and printed on desired flexible and stretchable substrates.^{2,6} Many functional devices have been fabricated and specifically a few photovoltaic devices have been demonstrated.^{7,8} To make stretchable electronics, elastomeric materials have been utilized in these approaches as basis to enable stretchability of the fabricated devices and specific designs have been considered to minimize the local strain at the brittle devices while maintaining the large stretchability of the devices as a whole. These designs include buckled devices,^{2,9} pop-up interconnects,^{4,8} and serpentine-shaped interconnects³ between functional devices that mitigate the local strain of these components through out-of-plane deformations (e.g., buckling and rotation). Despite the extraordinary success of these approaches in reaching functional devices with great flexibility and stretchability, the involvement of flexible and elastomeric substrates prevents the direction fabrication on them using mainstream manufacturing processes, such as

high-temperature processes like annealing and oxidation. The transfer printing on the other hand may also reduce the yield, particularly for thicker devices with large area.

Instead of using elastomeric substrates to make the device stretchable, there exists an alternative way to enable stretchability, which in fact has been around us since our childhood, namely, origami. As an art of paper folding, origami is to create three-dimensional structures from two-dimensional sheets through a high degree of folding along the creases. One of the central themes of origami is compactness and deformability of the folded structures, which has been recently explored for applications from space exploration (e.g., a foldable telescope lens¹⁰), to automotive safety (e.g., airbags), and biomedical devices (e.g., heart stent¹¹). Figure 1 shows an origami pattern by the name of Miura-ori,¹² where many identical parallelograms are linked through “mountain” and “valley” creases. Although the Miura-folding can be almost completely collapsed in one direction, the parallelograms remain undeformed. Thus, the deformability, particularly the stretchability of the Miura pattern as a whole is enabled through the folding and unfolding of the creases while maintaining the parallelograms rigid. This kind of origami pattern is called rigid origami, where the deformability

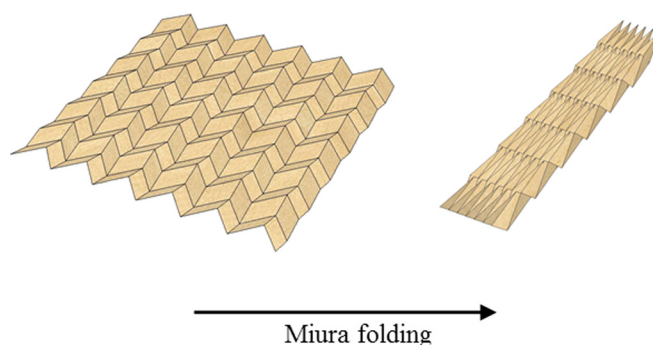


FIG. 1. Miura folding enables stretchability.

^{a)}Email: hanqing.jiang@asu.edu

^{b)}Email: hongyu.yu@asu.edu

is prescribed by the creases while the materials of making the origami pattern do not experience large strain except at the creases. Therefore, rigid origami provides an alternative way to enable deformability without using elastomeric materials.

In this Letter, we demonstrate the fabrication of stretchable electronics by utilizing rigid origami, without using elastomeric materials. Therefore, the fabrication processes to be presented here represent an example to utilize mainstream high-temperature processes to fabricate high-performance stretchable electronics. In this approach, high-performance functional devices are fabricated on rigid surfaces and do not experience large strain during deformation, and these rigid surfaces are joined by serpentine-shaped interconnects that allow for a full-degree folding and unfolding, which enables deformability. Specifically, we fabricate origami-enabled stretchable solar cells with metal traces embedded serpentine-shaped flexible polymers as interconnects to achieve unprecedented deformability. Over 600% areal compactness has been demonstrated. To bear localized strain at the creases, we utilize an innovative serpentine interconnect with hollow tubes as cushions to minimize the strain at the creases.¹³

The fabrication processes consist of two parts, namely the fabrication of the silicon (Si) solar cells and the origami structure (Fig. 2). The fabrication of the Si solar cells is standard and compatible with the mainstream high-temperature CMOS process. The detailed fabrication processes are described in the supplementary material.¹⁵ The top panel of Fig. 2 shows two fabricated Si solar cells on Si substrates, where two sets of serpentine shaped interconnects on top of Si wafer are utilized to connect rigid Si solar cells and the back illumination are used here. Then a Parylene-C layer is vapor-phase deposited using Parylene Deposition System (SCS PDS 2010). Parylene is the generic name of poly-para-xylylene, which can be conformally deposited at room temperature.¹⁴ The Parylene-C layer is then patterned using oxygen plasma (Oxford Instruments Plasmalab 80+ RIE) to open small rectangular windows ($10\ \mu\text{m} \times 50\ \mu\text{m}$ in size and $10\ \mu\text{m}$ apart between two windows) in rows along the central line of serpentine metal interconnects. In addition to patterning Parylene-C along interconnects, Parylene-C in the central area between Si solar cells are also patterned, which will form “a Parylene-C belt” to enhance the mechanical integrity of the solar cells with creases. These patterned windows in Parylene-C serve as the mask for Xenon difluoride (XeF_2) etching, a gas-phase isotropic Si etchant. The Si substrate is then undercut etched through these windows by XeF_2 , forming trenches underneath the serpentine metal interconnects and “Parylene-C belt”. These trenches function as cushions and have been found to reduce the localized stress at the serpentine structures.¹³ Deposition of another layer of Parylene-C ($15\ \mu\text{m}$ in thickness) is then conducted to conformally coat the trenches and form sealed Parylene-C microtubes underneath serpentine metal interconnects and “Parylene-C belt”. Finally, the Parylene-C on the top side is patterned by oxygen plasma to shape the outline of the device and open contact pads, followed by the backside deep reactive-ion etching (DRIE) (STS ICP Advanced Silicon Etch) using AZ 4620 photoresist as mask to release the origami Si solar cells.

Figure 3 shows the optical pictures of the fabricated solar cells at unfolded and folded states. The solar cells consist of

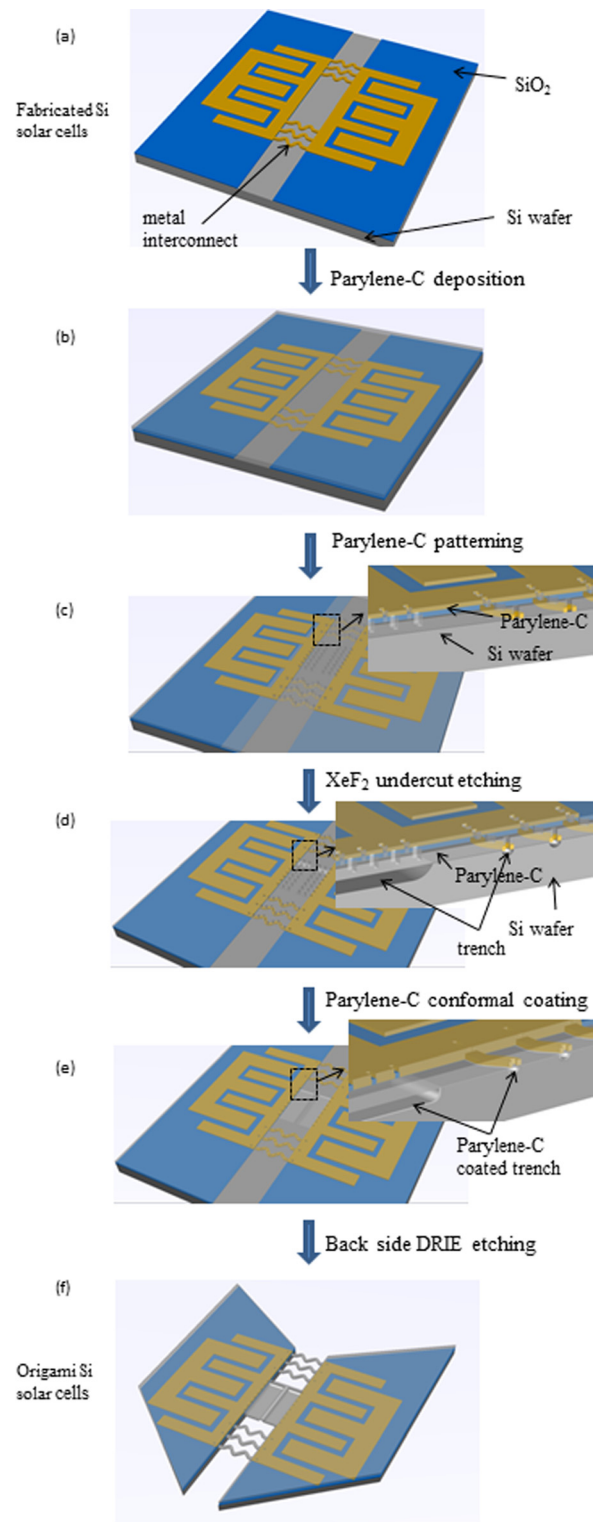


FIG. 2. Fabrication process of the origami structure for the deformable silicon solar cells. (a) Deposition of metal interconnects. (b) Deposition of first Parylene-C layer. (c) Pattern Parylene-C layer to form small rectangular holes as masks for XeF_2 undercut etching. (d) XeF_2 undercut etching Si substrate. (e) Coating of second layer of Parylene-C to seal the holes. (f) Backside Si etching leads to the final devices.

20 parallelograms that are electrically linked by metal traces embedded serpentine cables. Figure 3(a) shows the unfolded state with an inset of an optical micrograph of the serpentine cable. The size of each parallelogram is $1\ \text{cm}^2$ and the slit is $0.1\ \text{cm}$ in width. On each parallelogram, the active solar cell covers $0.2\ \text{cm}^2$, which leads to 20% areal coverage, which

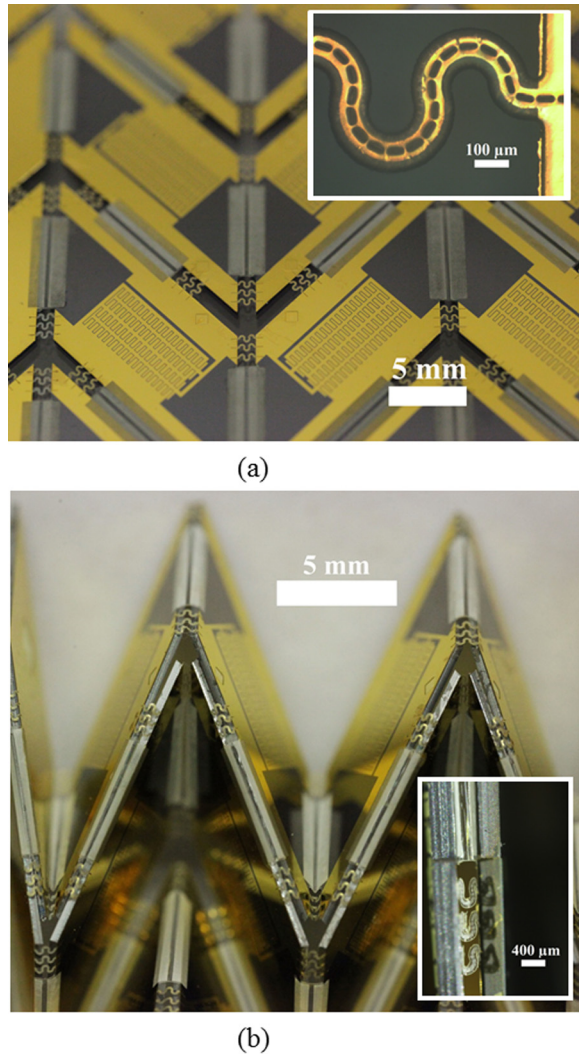


FIG. 3. Optical pictures of the fabricated origami-enabled Si solar cells, with (a) for unfolded state and (b) folded state. The insets show the metal traces embedded Parylene-C interconnects in serpentine shape.

can be significantly improved by optimized solar cell layout design. It is expected that 90% areal coverage can be reached. In the inset of Fig. 3(a), the etching holes for XeF_2 undercut etching are dark and the bright regions are gold traces due to the reflection of the light. The Parylene-C layer that encapsulates the metal traces cannot be clearly seen because of its transparency. Figure 3(b) shows the partially folded state and an optical micrograph as the inset confirms that the serpentine interconnect survives during folding, which is an important step to make stretchable solar cells using origami.

We demonstrate the stretchability of the origami based solar cells by defining linear compactness ε_{Linear} and areal compactness ε_{Areal} using the dimensions marked in Fig. 4 as

$$\varepsilon_{Linear}^x = \frac{L_x}{l_x} \text{ for } x\text{-direction,} \quad \varepsilon_{Linear}^y = \frac{L_y}{l_y} \text{ for } y\text{-direction,} \quad (1)$$

$$\varepsilon_{Areal} = \frac{L_x L_y}{l_x l_y} = \varepsilon_{Linear}^x \varepsilon_{Linear}^y. \quad (2)$$

Here L_x and L_y are dimensions for the completely unfolded state in x - and y -directions (Fig. 4(a)), respectively; and their

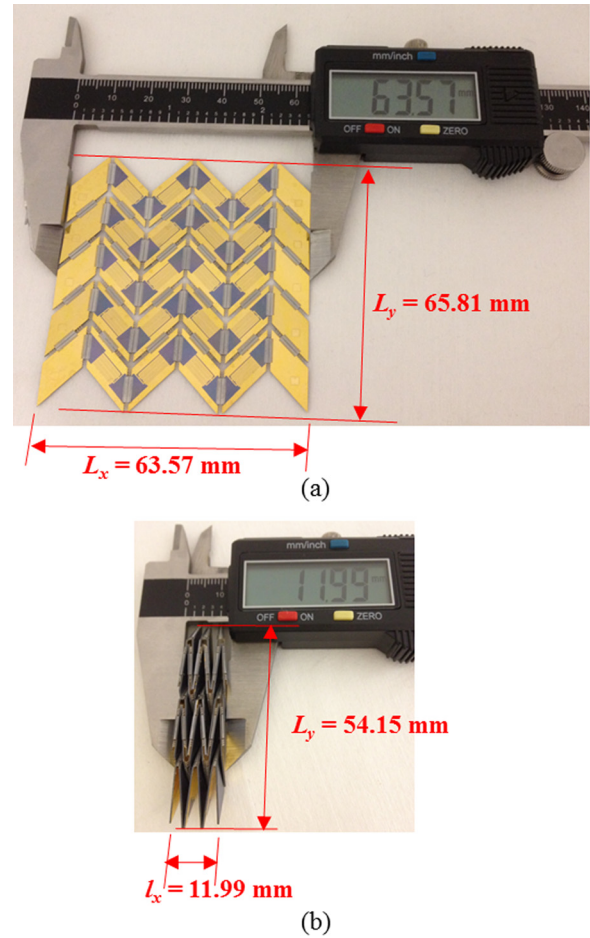


FIG. 4. Measured dimensions of the origami-enabled Si solar cells at (a) unfolded state and (b) completely folded state.

counterparts for the completely folded states are denoted by lower case letter “ l ” (Fig. 4(b)). Using the measured dimensions shown in Fig. 4, the origami-based solar cells have realized up to 530% linear compactness in x -direction and 644% areal compactness.

We characterize the performance of the origami solar cells with the emphasis on the behavior after cyclic folding and unfolding. A simulated AM1.5 spectrum with an intensity level of 100 mW/cm^2 is used during the current-voltage measurements and the tests are carried out using an Oriel[®] Sol2A Class ABA Solar Simulators (Newport). The intensity calibration (100 mW/cm^2) is achieved with a standard solar cell. The bias voltage is swept from -0.1 V to 0.5 V with 100 data points. Testing temperature is maintained at room temperature. Figure 5(a) shows the current density versus bias voltage plot for the solar cells at the original state (without folding) and after certain number of folding/unfolding. At the original state, the open circuit voltage (V_{oc}) is 0.455 V and the short circuit current density (J_{sc}) is 5.95 mA/cm^2 . The filling factor is 52.1%. The Si solar cell is then subjected to cyclic folding and unfolding up to 40 times. Video S1¹⁵ shows the cyclic folding and unfolding. It is observed that once the solar cell is folded, the short circuit current density starts to decrease and gradually saturates at around 4 mA/cm^2 after 10 cycles of folding/unfolding.

In comparison with unfolded state, there is about 30% reduction in short circuit current density after folding, which

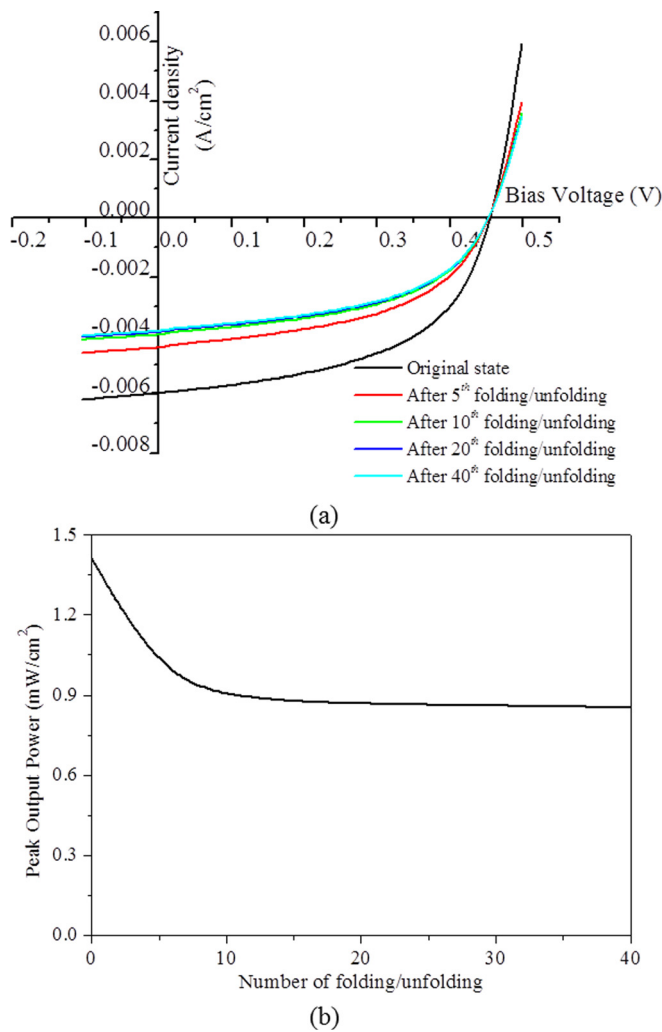


FIG. 5. Characterization of the origami-enabled Si solar cells. (a) Current density versus bias voltage for Si solar cells at original state and after cyclic folding and unfolding. (b) Peak output power versus number of folding and unfolding.

can be explained by the fracture of some interconnects. During the first few folding/unfolding, the creases between two parallelograms will gradually be formed and meanwhile some interconnects are fractured at these sites to initiate the formation of the creases. Once the creases are formed, further folding/unfolding just follows the defined creases and does not lead to new fracture at interconnects, which leads to a gradually saturated performance. As shown in Fig. 5(a), this reduction saturated even up to 40 times folding/unfolding. For the open circuit voltage (V_{oc}), it almost remains constant throughout 40 times folding/unfolding, which indicates that solar cells are not damaged since they are located on the rigid parallelograms. This explanation has been verified by an equivalent circuit model for the solar panel using PSPICE simulation software.

Figure 5(b) shows the maximum output power as a function of number of folding/unfolding. Similar trend is observed: the maximum output power drops after folding but gradually saturates after about 10 times folding/unfolding. We also noticed that V_{oc} (about 0.455 V) is lower than commercial Si solar cells (normally 0.5–0.7 V) because we only used $n+p$ junctions for simplicity instead of $p+-p-n+$ junctions that are

used in many commercial Si solar cells. We can readily adopt the commercial $p+-p-n+$ junctions in the origami-enabled stretchable solar cells, such as through ion-implantation that is completely compatible with the present process.

In summary, we have developed an alternative approach to fabricate stretchable electronics by utilizing origami. This approach does not involve elastomeric materials and is compatible with the mainstream CMOS process for high-performance devices. We have demonstrated an example of origami-enabled Si solar cells and showed that this solar cell can reach up to 644% areal compactness while maintain reasonable good performance upon cyclic folding/unfolding. This approach can be readily applied to other functional devices, ranging from sensors, displays, antenna, to energy storage devices.¹⁶ It is expected that this versatile approach can be seamlessly integrated with mature microelectronics process to fabricate functional devices that are able to survive combined stretching, compression, bending, and torsion, in both planar and curvilinear states, with heretofore unseen functionalities.

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